

| L Number | Hits | Search Text | DB | Time stamp |
|-------------|--------|---|---|---------------------|
| 1 | 100205 | (slot slit gap groove) with (pad paddle heat) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/03/03 11:04 |
| 2 | 285726 | (pad paddle heat) with (opening slit slot via grooves slots holes) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/03/03 11:05 |
| 3 | 35080 | (semiconductor die chip ic (integrated adj circuit)) same ((pad paddle heat) with (opening slit slot via grooves slots holes)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/03/03 11:07 |
| 4 | 204 | ((semiconductor die chip ic (integrated adj circuit)) same ((pad paddle heat) with (opening slit slot via grooves slots holes))) same (tiebar dambar ((dam tie) adj3 bar)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/03/03 11:08 |
| 5 | 171 | (leadframe lead (lead adj frame)) same (((semiconductor die chip ic (integrated adj circuit)) same ((pad paddle heat) with (opening slit slot via grooves slots holes))) same (tiebar dambar ((dam tie) adj3 bar))) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/03/03 11:09 |



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Records 1-2 of 2 In long Format

1. 2/34/1 (Item 1 from file: 351)

013054409 **Image available**

WPI Acc No: 2000-226274/200020

Thin plastic integrated circuit package for power or analog semiconductor devices has a die pad surrounded by leads from a leadframe and encapsulated leaving upper and lower surfaces of leads and die exposed

Patent Assignee: AMKOR TECHNOLOGY INC (AMKO-N); ANAM SEMICONDUCTOR INC (ANAM-N); ANAM SEMICONDUCTOR TECHNOLOGY CO LTD (ANAM-N); AMKOR TECHNOLOGY (AMKO-N)

Inventor: GLENN T P; JEWLER S J; MOON D H; ROMAN D; YEE J H; LEE J H

Number of Countries: 029 Number of Patents: 006

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---------------|------|----------|-------------|------|----------|--------|---|
| EP 989608 | A2 | 20000329 | EP 99305775 | A | 19990721 | 200020 | B |
| JP 2000150765 | A | 20000530 | JP 99325884 | A | 19991012 | 200033 | |
| KR 2000028854 | A | 20000525 | KR 9942950 | A | 19991005 | 200110 | |
| US 6281568 | B1 | 20010828 | US 98176614 | A | 19981021 | 200151 | |
| TW 429570 | A | 20010411 | TW 99116602 | A | 19990928 | 200157 | |
| US 6455356 | B1 | 20020924 | US 98176614 | A | 19981021 | 200266 | |
| | | | US 99395875 | A | 19990914 | | |

Priority Applications (No Type Date): US 98176614 A 19981021; US 99395875 A 19990914

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|-----------|------|-----|----|--------------|--------------|
| EP 989608 | A2 | E | 25 | H01L-023/495 | |

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

JP 2000150765 A 19 H01L-023/50

KR 2000028854 A H01L-023/50

US 6281568 B1 H01L-023/12

TW 429570 A H01L-023/495

US 6455356 B1 H01L-021/48

Div ex application US 98176614

Div ex patent US 6281568

Abstract (Basic): EP 989608 A2

NOVELTY - The package comprises a planar metal die pad (22) with an integrated circuit formed on a first side. Contact pads on the die are wire bonded to a number of leads (30). The package body is formed from an encapsulant material which covers the sides of the die pad and leads leaving the top and underside exposed.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) a metal leadframe for making an encapsulated integrated circuit package;

(b) a patterned metal strip for making a number of encapsulated integrated circuit packages;

(c) a method of making a package for an integrated circuit device.

USE - Packaging for an integrated circuit.

ADVANTAGE - Has numerous uses for e.g. power and analog devices in

a small size package. Leads can be placed closer to the die to minimize the length of the bond wire. The exposed second surface of the die pad can be connected by solder to the printed circuit board for package cooling.

DESCRIPTION OF DRAWING(S) - The figure shows a plan view of the leadframe used for making the package.

Metal die pad (22)

Leads (30)

pp; 25 DwgNo 2/16

Derwent Class: U11

International Patent Class (Main): H01L-021/48; H01L-023/12; H01L-023/495; H01L-023/50

International Patent Class (Additional): H01L-023/28

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2/34/2 (Item 2 from file: 345)

15806842

Basic Patent (No,Kind,Date): EP 989608 A2 20000329

PATENT FAMILY:

EUROPEAN PATENT OFFICE (EP)

Patent (No,Kind,Date): EP 989608 A2 20000329

PLASTIC INTEGRATED CIRCUIT DEVICE PACKAGE AND METHOD OF MAKING THE SAME (English; French; German)

Patent Assignee: AMKOR TECHNOLOGY INC (US); ANAM SEMICONDUCTOR INC (KR)

Author (Inventor): GLENN THOMAS P (US); JEWLER SCOTT J (US); MOON D H (KR); ROMAN DAVID (US); YEE J H (KR)

Priority (No,Kind,Date): US 176614 A 19981021

Applic (No,Kind,Date): EP 99305775 A 19990721

Designated States: (National) AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE

IPC: * H01L-023/495

Derwent WPI Acc No: * G 00-226274; G 00-226274

Language of Document: English

Patent (No,Kind,Date): EP 989608 A3 20010110

PLASTIC INTEGRATED CIRCUIT DEVICE PACKAGE AND METHOD OF MAKING THE SAME (English; French; German)

Patent Assignee: AMKOR TECHNOLOGY INC (US); ANAM SEMICONDUCTOR INC (KR)

Author (Inventor): GLENN THOMAS P (US); JEWLER SCOTT J (US); MOON D H (KR); ROMAN DAVID (US); YEE J H (KR)

Priority (No,Kind,Date): US 176614 A 19981021

Applic (No,Kind,Date): EP 99305775 A 19990721

Designated States: (National) AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE

IPC: * H01L-023/495

Derwent WPI Acc No: * G 00-226274

Language of Document: English

JAPAN (JP)

Patent (No,Kind,Date): JP 2000150765 A2 20000530

SEMICONDUCTOR INTEGRATED CIRCUIT PLASTIC PACKAGE, ULTRA- COMPACT LEAD FRAME FOR MANUFACTURE THEREOF, AND ITS MANUFACTURE (English)

Patent Assignee: AMKOR TECHNOLOGY INC; ANAM SEMICONDUCTOR INC

Author (Inventor): GLENN THOMAS P; JEWLER SCOTT J; ROMAN DAVID; YEE J H; D H MUN

Priority (No,Kind,Date): US 176614 A 19981021

Applic (No,Kind,Date): JP 99325884 A 19991012

IPC: * H01L-023/50; H01L-023/12; H01L-023/28

Derwent WPI Acc No: * G 00-226274
Language of Document: Japanese

KOREA, REPUBLIC (KR)

Patent (No,Kind,Date): KR 2000028854 A 20000525
PLASTIC INTEGRATED CIRCUIT DEVICE PACKAGE, MICRO LEAD FRAME AND
PRODUCING METHOD OF PACKAGE (English)
Patent Assignee: AMKOR TECHNOLOGY KOREA INC; AMKOR ELECTRONICS INC
Author (Inventor): GLEN THOMAS P (KR); JEWELLER SCOTT J (KR); ROMAN
DAVID (KR); LEE JAE HAK (KR); MUN DU WHAN (KR)
Priority (No,Kind,Date): US 176614 A 19981021
Applic (No,Kind,Date): KR 9942950 A 19991005
IPC: * H01L-023/50
Derwent WPI Acc No: * G 00-226274
Language of Document: Korean

UNITED STATES OF AMERICA (US)

Patent (No,Kind,Date): US 6281568 BA 20010828
PLASTIC INTEGRATED CIRCUIT DEVICE PACKAGE AND LEADFRAME HAVING
PARTIALLY UNDERCUT LEADS AND DIE PAD (English)
Patent Assignee: AMKOR TECHNOLOGY INC (US); ANAM SEMICONDUCTOR INC
(US)
Author (Inventor): GLENN THOMAS P (US); JEWLER SCOTT J (US); ROMAN
DAVID (US); YEE J H (KR); MOON D H (KR)
Priority (No,Kind,Date): US 176614 A 19981021
Applic (No,Kind,Date): US 176614 A 19981021
National class: * 257684000; 257666000; 257696000; 257698000;
257796000; 257675000; 257712000; 257713000; 257707000; 257711000;
257730000; 257788000
IPC: * H01L-023/12; H01L-023/28; H01L-023/50
Derwent WPI Acc No: * G 00-226274
Language of Document: English
Patent (No,Kind,Date): US 6455356 BA 20020924
METHODS FOR MODING A LEADFRAME IN PLASTIC INTEGRATED CIRCUIT DEVICES
(English)
Patent Assignee: AMKOR TECHNOLOGY (US)
Author (Inventor): GLENN THOMAS P (US); JEWLER SCOTT J (US); ROMAN
DAVID (US); YEE J H (KR); MOON D H (KR)
Priority (No,Kind,Date): US 395875 A 19990914; US 176614 A3
19981021
Applic (No,Kind,Date): US 395875 A 19990914
Addnl Info: 6281568 Patented
National class: * 438123000; 438124000; 438127000; 029827000;
029841000; 029855000
IPC: * H01L-021/48
Derwent WPI Acc No: * G 00-226274
Language of Document: English

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